Claims

1. A system for inspecting a defect of an electronic circuit pattern formed on a semiconductor wafer, comprising:

an inspection area setting unit which divides an area to be inspected into at least two partial inspection areas, each of which has different inspection conditions;

an inspection condition setting unit which sets inspection conditions for each partial inspection area that is set by the inspection area setting unit; and

an inspection executing unit which executes an inspection under the inspection conditions, which have been set by the inspection condition setting unit, for each partial inspection area set by the inspection area setting unit.

2. A system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection area setting unit divides the area to be inspected according to a layout pattern.

3. A system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection area setting unit divides the area to be inspected into a cell portion and a non-cell portion according to layout data.

4. A defect-inspection control system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection area setting unit comprises a display screen for overlaying at least one of a defect distribution map showing distribution of defect positions, a layout pattern, and a detected image of the area to be inspected, on an inspection area setting state, or for displaying at least

one of them and the inspection area setting state simultaneously.

5. A system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection area setting unit divides the area to be inspected into a defect output area and a non-output area; and the inspection executing unit outputs a defect, which exists in the defect output area set by the inspection area setting unit.

6. A defect-inspection control system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection area setting unit divides the area to be inspected into a cell portion and a non-cell portion, by referring to layout data;

the inspection executing unit detects an image of the cell portion having no defect, stores the image as a cell portion reference image, and detects an image for each position to be inspected, which is specified by a user, as a defect image;

in the non-cell portion, a position of an adjacent chip, which has the same pattern, is detected as a reference image for each of the positions to be inspected, and the defect image is compared with the reference image to extract a defect; and

in the cell portion, regardless of the position to be inspected, the defect image is compared with the reference image of the cell portion to extract a defect.

7. A system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection

area setting unit calculates a range of each function block included in an area to be inspected according to the layout data, in order to set the partial inspection areas.

8. A system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection area setting unit calculates distribution of wiring density in an area to be inspected according to the layout data, and divides the area to be inspected into areas, each of which has the same calculated wiring density, in order to set partial inspection areas.

9. A system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection area setting unit divides an area to be inspected into partial inspection areas, each of which has different criticality.

10. A system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection area setting unit displays a layout pattern of a whole chip on an inspection area setting screen, and registers an area, which has been specified by a user on the layout pattern, as the partial inspection area; or

a user edits the partial inspection area, which has been calculated by the inspection area setting unit, and registers the partial inspection area.

11. A system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection area setting unit superimposes each of the partial inspection areas on the layout pattern to display them.

12. A system for inspecting a defect of an electronic

circuit pattern according to claim 1, wherein the inspection area setting unit superimposes and displays at least two of: each of the partial inspection areas; the layout pattern; and a position where a defect occurred.

13. A system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection executing unit classifies detected defects by kind of defect; and

the inspection area setting unit superimposes a position on the layout pattern, where the defect occurred, on the layout pattern by using symbols, which are unique to kinds of defects, to display them.

14. A system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection executing unit classifies detected defects according to at least whether the defect is a true defect or a false report.

15. A system for inspecting a defect of an electronic circuit pattern according to claim 1, wherein the inspection area setting unit divides an area to be inspected into a cell portion and a non-cell portion;

in the cell portion, the inspection executing unit detects a defect image and a reference image and compares them to extract a defect; and

in the non-cell portion, the inspection executing unit detects only a defect image to detect a defect without detecting a reference image.

16. A system for inspecting a defect of an electronic circuit pattern formed on a semiconductor wafer, comprising:

an inspection condition setting unit which calculates peculiar inspection conditions for each position of an area to be inspected;

an inspection area setting unit which divides the area to be inspected into partial inspection areas, each of which has the same inspection conditions that are calculated by the inspection condition calculating unit; and

an inspection executing unit which executes inspection under the inspection conditions, which have been set by the inspection condition setting unit, for each partial inspection area set by the inspection area setting unit.

17. A defect-inspection control system for inspecting a defect of an electronic circuit pattern according to claim 16, wherein the inspection area setting unit comprises a display screen for overlaying at least one of a defect distribution map showing distribution of defect positions, a layout pattern, and a detected image of the area to be inspected, on an inspection area setting state, or for displaying at least one of them and the inspection area setting state simultaneously.

18. A system for inspecting a defect of an electronic circuit pattern according to claim 16, wherein the inspection area setting unit divides the area to be inspected into a defect output area and a non-output area; and

the inspection executing unit outputs a defect, which exists in the defect output area set by the inspection area setting unit.

19. A defect-inspection control system for inspecting a

defect of an electronic circuit pattern according to claim 16, wherein the inspection area setting unit divides the area to be inspected into a cell portion and a non-cell portion, by referring to layout data;

the inspection executing unit detects an image of the cell portion having no defect, stores the image as a cell portion reference image, and detects an image for each position to be inspected, which is specified by a user, as a defect image;

in the non-cell portion, a position of an adjacent chip, which has the same pattern, is detected as a reference image for each of the positions to be inspected, and the defect image is compared with the reference image to extract a defect; and

in the cell portion, regardless of the position to be inspected, the defect image is compared with the reference image of the cell portion to extract a defect.

20. A system for inspecting a defect of an electronic circuit pattern formed on a semiconductor wafer, comprising:

a defect extracting unit which determines coordinates of a defect position on the semiconductor wafer, and an attribute;

an inspection area setting unit which divides an area to be inspected into a plurality of partial inspection areas, each of which has a different defect control criterion;

a defect control criterion setting unit which sets a defect control criterion for each of the partial inspection areas, each of which has a different defect control criterion;

and

a defect classification unit which gives control information to the defect position coordinates, which have been determined by the defect extracting unit, for each defect according to the defect control criterion set by the defect control criterion setting unit, and an attribute of the defect.

21. A defect-inspection control system for inspecting a defect of an electronic circuit pattern according to Claim 20, wherein the defect extracting unit calculates at least coordinates of a defect position, and a size of a defect;

the defect control criterion setting unit calculates a critical defect judgment size at each position of the area to be inspected according to layout data; and

the defect classification unit compares a defect size with the critical defect judgment size, which has been set by the control criterion setting unit, for the defect position coordinates calculated by the defect extracting unit, and gives control information, which indicates whether or not it is critical, to each defect.

22. A method for inspecting a defect of an electronic circuit pattern, comprising:

a process for reading layout data of an electronic circuit pattern;

a process for dividing an inspection area of the electronic circuit pattern into a plurality of inspection areas according to the read layout data;

a process for setting inspection conditions, which

correspond to each inspection area, for each of the plurality of divided inspection areas;

a process for picking up the electronic circuit pattern to acquire an image of the electronic circuit pattern;

a process for inspecting each of the inspection areas for the acquired image, using the inspection conditions that are set for each of the inspection areas; and

a process for displaying a result of the inspection on a screen.

23. A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein in the process for dividing an inspection area into a plurality of inspection areas, the inspection area is divided into the plurality of inspection areas, each of which has different density of the electronic circuit pattern.

24. A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein the layout pattern, which has been divided into the plurality of layout patterns, is displayed on a screen.

25. A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein the layout pattern, which has been divided into the plurality of layout patterns, is identified for each divided area, and is displayed on a screen.

26. A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein in the process for dividing an inspection area into a plurality of inspection areas, a range of each function block included in an area to

be inspected is calculated according to the layout data, and thereby the inspection area is divided into the function blocks.

27. A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein in the process for dividing an inspection area into a plurality of inspection areas, distribution of wiring density in an area to be inspected is calculated according to the layout data, and thereby the area to be inspected is divided into areas, each of which has the same calculated wiring density.

28. A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein in the process for dividing an inspection area into a plurality of inspection areas, an inspection area is divided into areas, each of which has different criticality.

29. A method for inspecting a defect of an electronic circuit pattern according to Claim 22, wherein in the process for dividing an inspection area into a plurality of inspection areas, a layout pattern of a whole chip is displayed on a screen, in addition to it, the layout pattern is divided into areas, each of which has been specified by a user, and then the areas are registered.

30. A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein in the process for dividing an inspection area into a plurality of inspection areas, the inspection area, which has been divided into the plurality of inspection areas, is superimposed on the layout pattern to display them.

31. A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein in the process for dividing an inspection area into a plurality of inspection areas, from among the inspection area, which has been divided into the plurality of inspection areas, the layout pattern, and a position where a defect occurred, at least two of them are superimposed to display them.

32. A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein in the process for inspecting each of the inspection areas, detected defects are classified by kind of defect; and

in the process for displaying a result of the inspection on a screen, a defect occurrence position on the layout pattern is superimposed on the layout pattern to display them, using symbols, which are unique to kinds of defects.

33. A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein in the process for inspecting each of the inspection areas, detected defects are classified according to at least whether the defect is a true defect or a false report.

34. A method for inspecting a defect of an electronic circuit pattern according to claim 22, wherein in the process for dividing an inspection area into a plurality of inspection areas, an area to be inspected is divided into a cell portion and a non-cell portion; and

in the process for inspecting each of the inspection areas, in the cell portion, a defect image and a reference image are detected and compared with each other to extract a

defect, whereas in the non-cell portion, only a defect image is detected to detect a defect without detecting a reference image.

35. A method for inspect a defect of an electronic circuit pattern, comprising:

a process for reading position information about a defect of an electronic circuit pattern formed on a substrate, which has been detected by the defect detection unit and stored in a first storage unit;

a process for reading layout data of an electronic circuit pattern formed on a substrate from a second storage unit;

a process for creating a layout pattern from the read layout data;

a process for dividing an electronic circuit pattern formed on the substrate into a plurality of areas, using the created layout pattern;

a process for setting image acquisition conditions for each of the plurality of divided areas;

a process for picking up the electronic circuit pattern to acquire an image of the defect of the electronic circuit pattern, according to the read position information about the defect of the electronic circuit pattern, and the image acquisition conditions that have been set for each of the plurality of areas; and

a process for displaying an image of the acquired defect on a screen.

36. A method for inspecting a defect of an electronic

circuit pattern according to claim 35, wherein in the process for setting image acquisition conditions, a plurality of image acquisition conditions are set for each area.

37. A method for inspecting a defect of an electronic circuit pattern according to claim 35, wherein in the plurality of image acquisition conditions, a condition of image magnification of the electronic circuit pattern, which should be acquired, is included.

38. A method for inspecting a defect of an electronic circuit pattern according to claim 35, wherein in the process for acquiring an image of the electronic circuit pattern, a process for acquiring a reference image at a position corresponding to a position of a defect, of which an image is acquired, is also included.

39. A method for inspecting a defect of an electronic circuit pattern according to claim 35, wherein in the process for displaying an image of a defect on a screen, the image of the defect is classified, and is displayed on the screen.

40. A method for inspecting a defect of an electronic circuit pattern according to Claim 35, wherein in the process for dividing an electronic circuit pattern into a plurality of areas, the plurality of areas are divided into a plurality of areas in response to density of the electronic circuit pattern.